## LIST OF THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

What is claimed is:

Claims 1-16 (canceled).

Claim 17 (Previously presented):A non-volatile memory structure comprising:

a substrate;

a plurality of gate dielectric layers disposed on the substrate, wherein at least one hetero element is planted on the top layer of the gate dielectric layers so as to provide an increased electron trapping density in the gate dielectric layers;

a gate electrode layer formed on the top of the gate dielectric layers; and a source/drain electrode formed at the substrate on both sides of the gate dielectric layer.

Claim 18 (Previously presented): the non-volatile memory structure as claimed in claim 17, wherein the gate dielectric layers including a first oxide layer, a nitride layer, and a second oxide layer.

Claim 19 (Previously presented): the non-volatile memory structure as claimed in claim 17, wherein the gate dielectric layers comprises at least one layer made of silicon carbide.

Claim 20 (Previously presented): the non-volatile memory structure as claimed in claim 17, wherein the gate dielectric layers comprises at least one layer made of aluminum oxide (Al2O3).

Claim 21 (Previously presented): the non-volatile memory structure as claimed in claim 17, wherein the at least one hetero element is selected from a group consisting of germanium, silicon, nitrogen, or oxygen.

Claim 22 (Previously presented): the non-volatile memory structure as claimed in claim 17, wherein the gate dielectric layers including a first silicon dioxide layer, a silicon nitride layer, and a second silicon dioxide layer.

Claim 23 (Previously presented): a non-volatile memory structure comprising:

a plurality of gate dielectric layers disposed on a substrate, said gate dielectric layers comprising a first dielectric layer formed on the substrate, a second dielectric layer formed on said first dielectric layer, and a third dielectric layer formed on said second dielectric layer, said first dielectric layer and said second dielectric layer are different materials, wherein at least one hetero element is planted on the third dielectric layer for increasing electron trapping density in the gate dielectric layers;

a gate electrode layer formed on said plurality of gate dielectric layers; and

a source/drain electrode formed at said substrate on both sides of said plurality of gate dielectric layers.

Claim 24 (Previously presented): the non-volatile memory structure as claimed in claim 23, wherein said first dielectric layer including a first oxide layer and said second dielectric layer comprising a nitride layer.

Claim 25 (Previously presented): the non-volatile memory structure as claimed in claim 23, wherein said first dielectric layer and said third dielectric layer are same material.

Claim 26 (Previously presented); the non-volatile memory structure as claimed in claim 23, wherein said at least one hetero element is germanium.

Claim 27 (Previously presented); the non-volatile memory structure as claimed in claim 23, wherein said at least one hetero element is silicon.

Claim 28 (Previously presented): the non-volatile memory structure as claimed in claim 23, wherein the gate dielectric layers comprises at least one layer made of silicon carbide.

Claim 29 (Previously presented): the non-volatile memory structure as claimed in claim 23, wherein the gate dielectric layers comprises at least one layer made of aluminum oxide (Al2O3).

Claim 30 (Previously presented): the non-volatile memory structure as claimed in claim 23, wherein said at least one hetero element is selected from a group consisting of germanium, silicon, nitrogen, or oxygen.

Claim 31 (Previously presented): the non-volatile memory structure as claimed in claim 23, wherein the gate dielectric layers including a first silicon dioxide layer, a silicon nitride layer, and a second silicon dioxide layer.

Claim 32 (Cancelled)

Claim 33 (Cancelled)